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MERGED ARRAY CONTROLLER WITH PROCESSING ELEMENT

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This application is a continuation of U.S. Serial No. 09/783,156 filed February 14, 2001, now issued U.S. Patent No. 6,606,699, which is a continuation of U.S. Serial No. 09/169,072 filed October 9, 1998, now issued U.S. Patent No. 6,219,776, which claims the benefit of provisional application Serial No. 60/077,457 filed March 10, 1998, all of which are hereby incorporated by reference in their entirety.

Field of the Invention

The present invention relates generally to improvements to array processing, and more particularly, to advantageous techniques for providing dual mode operation of a processor as both a control element for an array and as a processing element in the array.

Background of the Invention

Separate control and processing elements are seen in a variety of parallel processing arrays. Such elements are typically dedicated to defined control or processing tasks. Various aspects of such arrangements result in overall system inefficiencies.

Summary of the Invention

The present invention recognizes that typically in the prior art when a Single Instruction Multiple Data stream (SIMD) instruction is executed, only the array's Processing Element's (PE's) resources are used, except for the controller Sequence Processor's (SP's) address generation resources, and when a Single Instruction Single Data (SISD) instruction is executed, only the controller SP's resources are used thereby keeping the controller resources separate from the SIMD array resources. The present invention advantageously combines a PE and the controller SP into a single device, eliminates a dedicated PE-to-SP data bus by taking advantage of this fact, and allows the combined unit to share a single set of execution units thereby reducing implementation costs. With the present invention, an SP controller SISD instruction can be executed in parallel with a SIMD PE instruction.

These and other features, aspects and advantages of the invention will be apparent to those of skill in the art from the following detailed description taken together with the accompanying drawings.

Brief Description of the Drawings

Fig. 1 illustrates an SIMD array of PEs controlled by a controller SP with a dedicated PE-to-SP data bus;

Further details of a presently preferred ManArray architecture which may be utilized in conjunction with the present invention are found in United States Patent Application Serial Nos. 08/885,310 and 08/949,122 filed June 30, 1997 and October 10, 1997, now issued U.S. Patent No. 6,023,753 and 6,167,502, respectively, Provisional Application Serial No. 60/064,619 entitled Methods and Apparatus for Efficient Synchronous MIMD VLIW Communication" filed November 7, 1997, Provisional Application Serial No. 60/067,511 entitled "Method and Apparatus for Dynamically Modifying Instructions in a Very Long Instruction Word Processor" filed December 4, 1997, Provisional Application Serial No. 60/068,021 entitled "Methods and Apparatus for Scalable Instruction Set Architecture" filed December 18, 1997, Provisional Application Serial No. 60/071,248 entitled "Methods and Apparatus to Dynamically Expand the Instruction Pipeline of a Very Long Instruction Word Processor" filed January 12, 1998, Provisional Application Serial No. 60/072,915 entitled "Methods and Apparatus to Support Conditional Execution in a VLIW-Based Array Processor with Subword Execution filed January 28, 1988, and Provisional Application Serial No. 60/088,148 entitled "Methods and Apparatus for ManArray PE-PE Switch Control" filed on June 5, 1998, and Provisional Application Serial No. 60,092,148 entitled "Methods and Apparatus for Dynamic Instruction Controlled Reconfigurable Register File with Extended Precision" filed on July 9, 1998, and Provisional Application Serial No. 60/092,130 entitled "Methods and Apparatus for Instruction Addressing in Indirect VLIW Processors" filed on July 9, 1998, all of which are assigned to the assignee of the present invention and incorporated herein by reference in their entirety.

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In one aspect, the present invention provides a dynamic merging processor (DP) capable of dynamically supporting two independent modes of operation and a third unique combined mode of operation in a highly parallel processor comprising an array of processing elements. The third combined mode of operation can be used on highly parallel processors with a very long instruction word (VLIW) architecture given this invention. Dynamically changing modes of operation is defined as modes that can be changed cycle by cycle under programmer control. A combined mode of operation means that in any cycle the two independent modes of operation can be in effect governed by the indirect VLIW (iVLIW) architecture. In a first mode of operation, the DP acts as one of the processing elements in the array and participates in the execution of single-instruction-multiple-data (SIMD) instructions. In a second mode of operation, the DP acts as the controlling element for the array and executes single-instruction-single-data (SISD) instructions. In the third mode of operation, the DP acts simultaneously as the controlling element for the array and as one of the processing elements in the array. This is accomplished when the DP executes an iVLIW